Joint implementation of the sharing OTA and bias current regulation techniques in a 11-bit 10 MS/s pipelined ADC

Jose Á. Díaz-Madrid[1], Ginés Doménech-Asensi[2],
José J. Martínez-Álvarez[2], Juan Zapata-Pérez[2], Ramón Ruiz-Merino[2]
[1]Dpto. de Integracion, Centro Universitario de la Defensa, Universidad Politecnica de Cartagena.
c/ Coronel Lopez Pena, 30720, Santiago de la Rivera, Murcia, Spain.
[2]Universidad Politécnica de Cartagena, Plaza del Hospital, 1, 30202, Cartagena, Spain

Abstract

The power dissipation of a pipeline analog to digital converter (ADC) depends on different design strategies. In this brief communication, an 11-bit pipeline ADC consisting of five stages with 2.5 effective bit resolution is described. The circuit combines two main techniques to improve power dissipation, such as sharing OTAs between adjacent ADC stages and dynamic regulation of the OTA biasing according to the stage and subcycle of operation. To reduce the charge injection effect caused by the OTA sharing added circuitry, the ADC uses a topology based on four-input OTAs to reduce the number of transmission gates. The ADC has been fabricated using a standard 0.35 μm CMOS process. It consumes 17.85 mW at 10 MSample/s sampling rate. With this resolution and sampling rate, the measurement results show that it achieves 58.20 dB SNDR and 9.38 bit ENOB at 1 MHz input frequency.

Keywords— Analog-to-digital converter (ADC), Op-amp sharing, Bias current regulation, Low power

1 Introduction

Power dissipation is a key specification in modern portable electronic devices. For those containing a digital camera, pipelined ADCs in the range of 8 to 12 bits are the type of data converter usually used [7]-[28]. So, several techniques have been developed to reduce the power dissipation in these types of circuits. A pipelined ADC is composed of several cascaded stages, each one usually providing a 2-bit or 3-bit output, which contribute to the final output digital word [9]. Stage resolution of the ADC stages affects the circuit power performance and different comparative studies [14]-[25] conclude that the optimal solution does not necessarily follow the strategy of using the lowest possible resolution per stage. Also, each stage is composed of several circuits and sub-circuits, the operational amplifier being the one which consumes more power. So, a lot of effort has been made to cut down the power dissipation due to this circuit. Power reduction has been traditionally achieved exploiting stage scaling techniques [18] - [6], where the sizing of the switched capacitor (SC) circuits in each stage are determined by noise requirements. Given that thermal noise contribution of a given stage is reduced by the previous stage gain, the capacitor size is reduced in each cascaded stage. So, the bias current of the amplifiers can also be consequently scaled down. Another approach is based on the fact that each stage is only amplifying half of the conversion cycles. So, the same amplifier can be used alternatively by adjacent stages working in opposite clock phases [29] - [2]. Although this technique reduces the number of amplifiers by half, the same proportion of power dissipation on the whole circuit is not reduced since this configuration requires additional transmission gates to control the signal flow. However, this technique can still be improved, given that the OTA power consumption is not optimized for a single stage as it is shared between two of them. So, the OTA is normally oversized in power consumption with respect to the second shared stage requirements. In [17] a technique to solve this oversizing employing parallel OTA scaling, was proposed. However, this technique required an increase in the number of OTAs in each stage. In this paper, the prototype and measured performance of an ADC implementing an alternative technique to adapt the power consumption of the shared OTA to the requirements of each stage are described. The advantage of this approach is that it reduces the number of operational amplifiers compared to [17] while performing the same functionality of bias regulation. The circuit has been prototyped and tested following the biasing technique described in [11]. The main novelty is the implementation of the adaptive bias current and sharing OTA techniques at the same time. This allows for the adaption of the current according, not only to each OTA, but also to the subcycle and active stages. The circuit also includes a modified dynamic comparator structure with very low kick-back noise. Moreover, to reduce the charge injection effect caused by

the OTA sharing added circuitry, the ADC uses a topology based on four-input OTAs to reduce the number of transmission gates. The rest of the paper is organized as follows. Section 2 describes the architecture of the prototyped circuit, while the implementation of the transconductance amplifier is detailed in 3. Results from circuit measurements are shown in Section 4. Finally, conclusions are drawn in Section 5.

2 ADC architecture

Fig. 1 shows the structure of the 11-bit pipeline ADC. The circuit is composed of four stages which share two OTAs and a fifth stage which is basically a flash ADC.

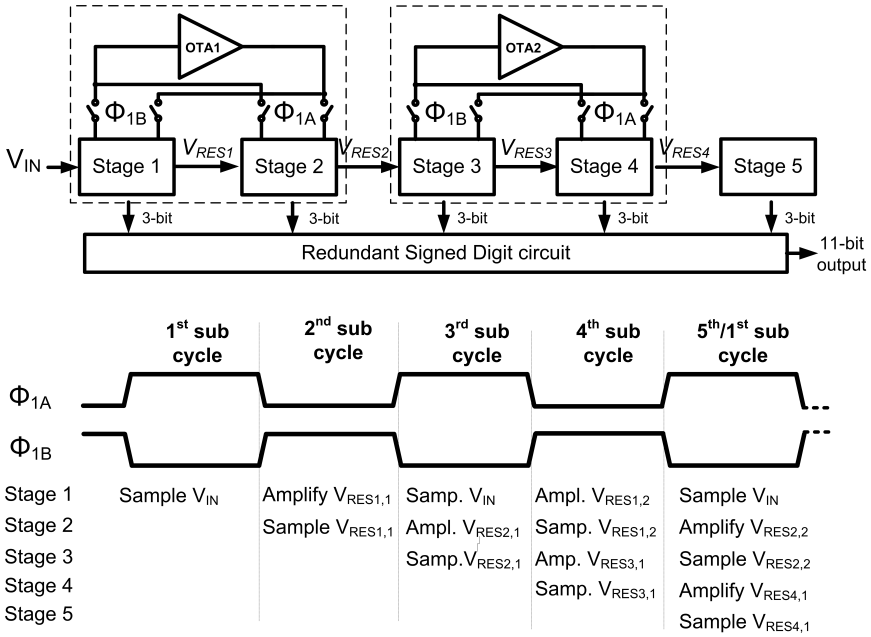

Figure 1: Structure of the 11-bit 5 stages pipelined ADC with shared OTA between adjacent stages

Every stage provides a 3-bit digital output to feed a digital circuit implementing a Redundant Signed Digit (RSD) algorithm [3]. The output from this circuit is the final 11 bit digital code. Given that even and odd stages work in opposite clock signals, and that each stage is amplifying only half of the time, a common OTA can be shared between two adjacent stages. During the first subcycle V_{IN} is sampled by the first stage, whose internal flash DAC outputs a three-bit digital word. In the second subcycle, the first stage amplifies the residue value and outputs $V_{RES1,1}$, which is sampled by stage 2. Simultaneously, the internal DAC of stage 2 provides a three bit digital word. In the figure, $V_{(RESi,t)}$ represents the residue value of stage i at sampled time t. The process continues until stage 5 samples $V_{RES4,1}$ and outputs its digital word. So, it takes 5 sub cycles to complete a whole conversion. Fig. 2 shows a simplified structure of the two first stages of the ADC. In order to clarify the figure, it represents single ended circuits, although the real converter has been synthesized using a fully differential configuration to improve the common mode rejection ratio (CMRR).

As described in the previous section, each stage works in two subcycles. During the first subcycle, the first stage samples the input voltage V_{IN}, charging capacitors C_{s1} and C_{f1}. At the same time, this value is taken to the group of six comparators CMP1 which feed the decoder ($DEC1$), to produce a 3-bit stage digital output $D = (D2, D1, D0)$ as well as control signals to charge capacitors C_{s1}. During the second subcycle, the OTA is used to produce the output voltage, called residue voltage (V_{RES}), given by:

$$V_{RES} = 4 \cdot V_{IN} + D \cdot V_{REF} \tag{1}$$

The residue voltage is simultaneously sampled by the second stage, charging capacitors C_{s2} and C_{f2}. Also, decoder DEC is fed by comparators CMP2 and produces a 3-bit digital output ($D5, D4, D3$) and control signals to charge capacitors C_{s2}. This two-stage process is repeated during the third and fourth subcycles, taking the amplified output from the second stage as input to the third stage. Thus, the OTA is working in every subcycle, while transmission gates TG1 and TG2 select which one of both stages is amplifying. The fifth stage contains only the comparators and the decoder, since no amplification is required. All the stages work in a pipelined operation, as shown in the timing diagram of Fig. 1 Although this topology seems efficient from an architectural perspective, transmission gates TG1 and TG2 add charge injection to the circuit, which contributes to non-linearity effects that penalize the SNDR of the ADC. Moreover, since the same OTA is used by two adjacent stages, it consumes the same power regardless of the stage which is using it. So, in order to achieve the settling time specifications

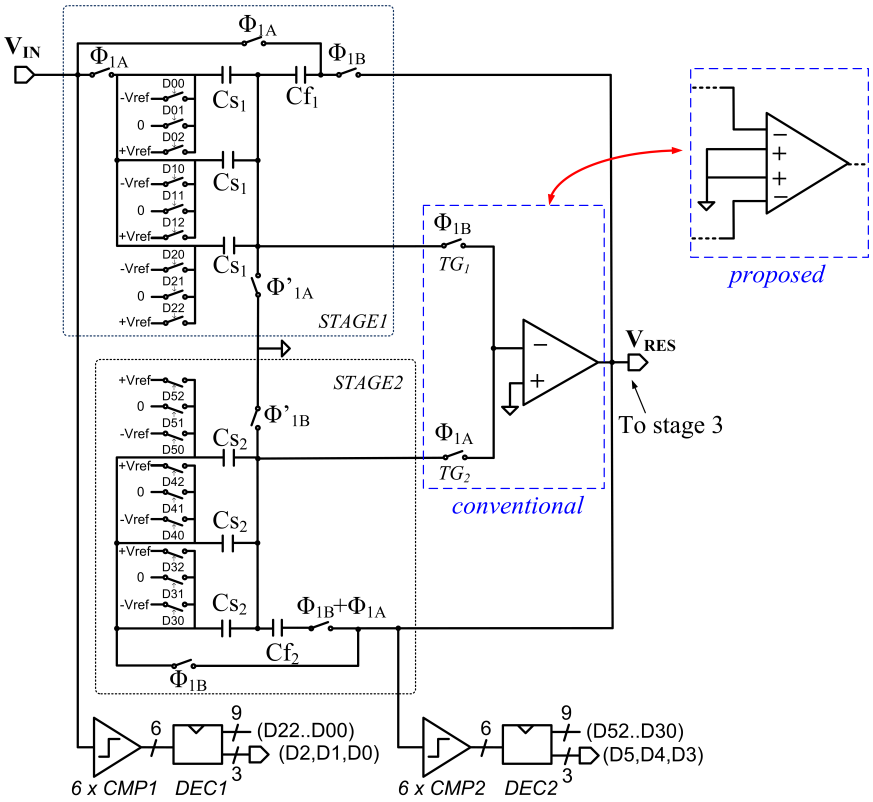

Figure 2: Conventional schematic of two stages with a shared OTA and proposed circuit with a four-input OTA.

for both stages, given that the load capacitance of the first stage is larger that that of the second one, when the second stage is amplifying, the OTA is over biased. The architecture proposed in this paper to deal with these two effects is shown in Fig. 2. Compared to the conventional implementation, the two-input OTA has been replaced by a four-input one. This allows the removal of the transmission gates TG1 and TG2 and so, it reduces the charge injection effect. Moreover, the OTA includes a bias regulation circuitry which varies the amplifier biasing current according to the ADC subcycle of operation. In order to reduce the noise generated by the dynamic comparators, in this work comparators CMP1 and CMP2 used low kick-back noise circuits [10].

3 Transconductance amplifier

The structure of the four input OTA is shown in Fig. 3 [11]. Due to the requirements of the ADC, a telescopic OTA with gain boosting [16] has been used.

This architecture offers a high DC-gain, a high unity gain bandwidth and a fast settling time, thanks to the pair of gain boosting amplifiers A1 and A2. The input differential pairs made from devices M1 and M2 are connected to stage 1 and stage 2 respectively. The biasing of the first one is primarily driven by device M9. Compared to a conventional amplifier, the OTA in the figure includes three additional subcircuits to regulate the biasing current depending on the subcycle of operation. Also, a second switched-capacitor common mode feedback circuit (CMFB), connected to devices M3 and M4 is added in order to achieve a fast regulation of the common mode (CM) voltage. Fig. 4 shows the structure of the CMFB used to set the output CM voltage in the amplifier. A CMFB circuit consists of a CM sense-detect circuit and a comparison circuit. In a switched-capacitor CMFB the capacitors are precharged to the reference voltage $V_{CM,ref}$ and then the OTA output voltages $Vout^+$ and $Vout^-$ are level-shifted by $V_{CM,ref}$ and leveraged to generate the desired output voltage $V_{CM,out}$. A detailed description of this circuit can be found in [8].

When the ADC stage 1 is amplifying, control signal ϕ_{1B} is high while ϕ_{1A} and $\overline{\phi}_{1B}$ are low. Thus, the OTA differential pair M2 is disabled allowing the two CMFBs to regulate the common mode with the maximum bias current and consequently obtain the highest slew rate. The bias current flows through M9 and M10-M11 in parallel to M12. In the PMOS side, devices M5 are ON and current flows through M3-M5 in parallel to M4. In the next subcycle, when stage 2 is amplifying signal ϕ_{1B} is low and signals ϕ_{1A} and $\overline{\phi}_{1B}$ are high. So, the differential pair M1 is disabled. The current mirrors formed by the transistors (M11-M17) and (M13-M3) are also disabled and the bias current flows only through M8 and M12. Concerning the PMOS devices, M5 is OFF and current flows only through devices M4. Thus, by means of the transistors M5, M8, M9 and M10, the OTA

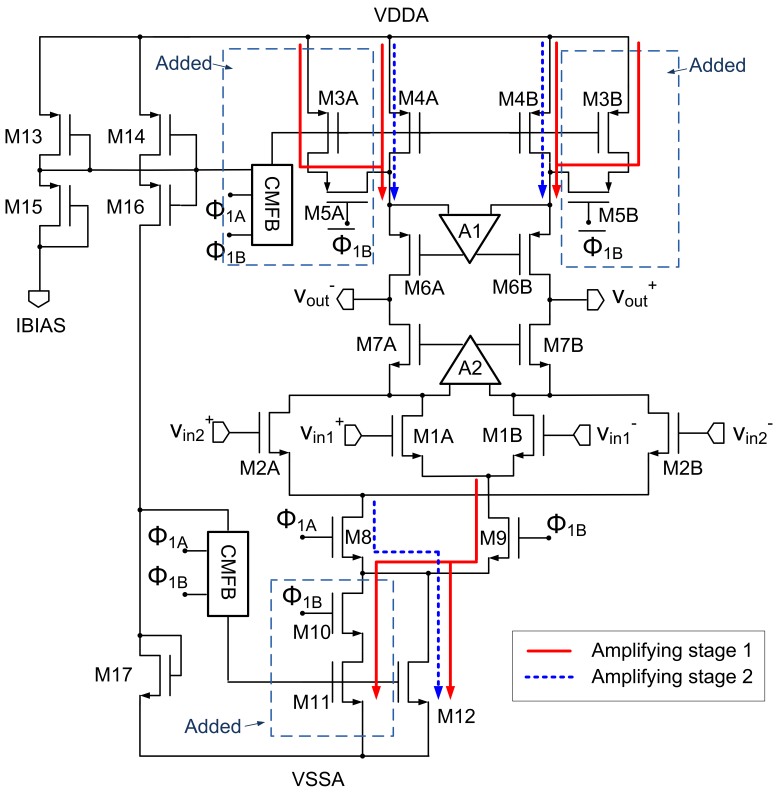

Figure 3: Four inputs OTA with adaptive bias current circuitry for stage 1.

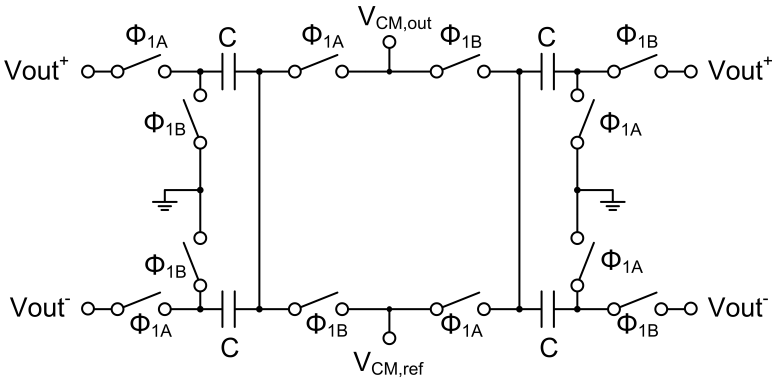

Figure 4: Structure of the switched capacitor common mode feedback circuit.

adapts the power consumption to the requirement of the active amplifying stage. This technique is better than alternatively switching on and off the OTA bias currents in two parallel branches, one for the biasing of the first stage amplification and a smaller one for the second stage amplification, because this last option would require the switching of larger currents, causing a negative impact on the dynamic behaviour of the circuit. The proposed technique implies that there is a permanent current biasing the OTA and when a larger value is required, only the difference is supplied through the mentioned biasing device, which improves the dynamic behaviour of the biasing circuit. Given that the control signals driving these devices (ϕ_{1A}, ϕ_{1B} and $\overline{\phi}_{1B}$) are the same as the control signals used in the CMFB circuits, a full synchronization is achieved. The OTAs have been scaled to reach an efficient ADC from the point of view of the power consumption and area. The size of the gain boosting OTAs, A1 and A2 depends also on the stage in which they are implemented. Fig. 5 shows the internal structure of these circuits.

Amplifiers shown in Fig. 5.a and Fig. 5.b. correspond, respectively, to gain-boosting amplifiers A1 and A2 in Fig. 3. These amplifiers have been designed implementing a symmetrical configuration with cascode transistors. The cascode transistors enhance the DC gain of the shared OTA to reach the requirements of the stage 1 and 2. Given that the gain boosting OTAs corresponding to the shared OTA between stage 3 and 4 need a lower DC gain, their topology was simplified removing the cascode transistors (Fig. 5.c Fig. 5.d). This allows a reduction of the power consumption of these stages.

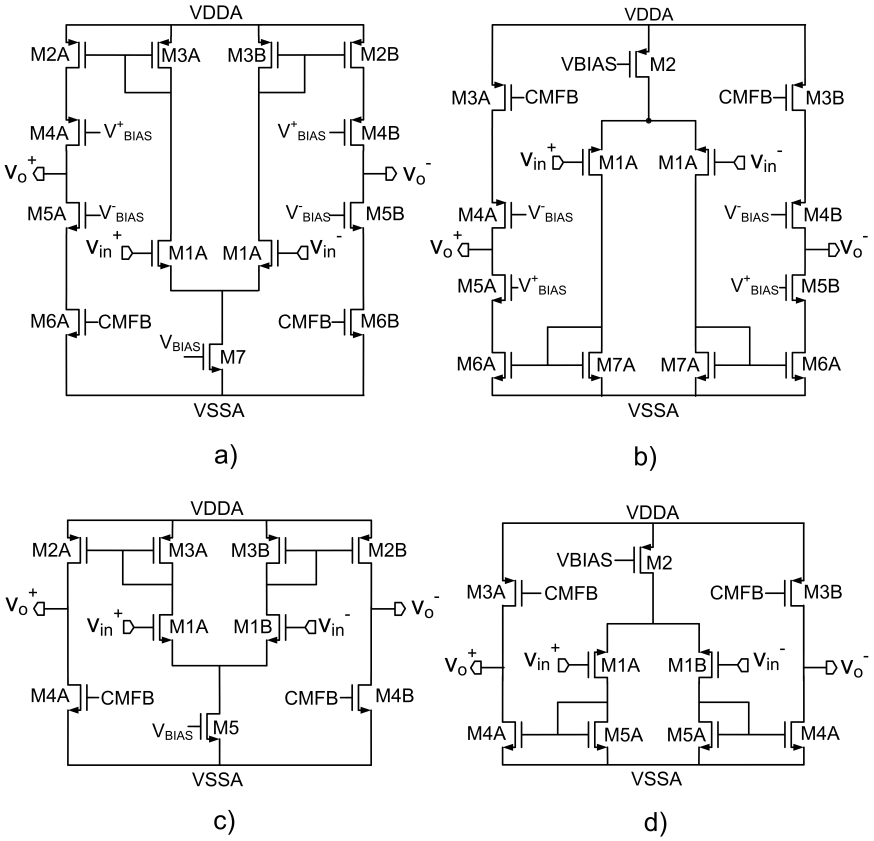

Figure 5: Gain Boosting OTAs with cascode transistors for OTA1 and OTA 2.

Table 1: Capacity values in the ADC and bias and total currents in the two OTAs with a sampling period of 50 ns

Stage	C_s (fF)	C_f (fF)	C_{other} (fF)	C_L (fF)	Est. I_{Bias} (μA)	I_{Bias} (μA)	I_{Total} (μA)
1	780	260	2500	3360	2016	2048	3000
2	450	150	1600	2230	1234	1335	2280
3	360	120	1400	1980	1180	1508	1959
4	195	65	1000	1065	640	630	1080

4 Measurements results

Fig. 6 shows a micrograph of the prototyped pipeline ADC. The circuit has been prototyped in a standard CMOS 0.35μm process from AMS. The size is 1130 x 840μm^2. The bias current of each OTA has been sized according to the slew rate requirements for each stage n and its capacitive load $C_{L,n} = C_{f,n} + C_{s,n+1} + C_{f,n+1} + C_{others,n}$, where C_{others} is an estimation of the input capacitor of the dynamic comparators, OTAs, transmission gates and the parasitic capacitors. On the other hand, for a sampling period of 100 ns the settling time for the amplification process has been set to 50 ns. So, for a full output voltage range of $3V_{pp}$ and a rise time of 5 ns, (10% of 50 ns), the slew rate is 600 V/μs. According to these values, the real values of the biasing current I_{Bias} (estimated and actual) and total current I_{Total} are those shown in Table 1.

Different simulations [11] and measurements have been performed to evaluate the circuit performance. Fig. 7 shows the evolution of the total bias current per OTA over time. The current consumed by OTA 1 changes between 3 mA, when stage 1 is amplifying, to 2.28 mA when the amplification is done on stage 2. Similarly, the bias current for OTA 2 changes between 1.96 mA and 1.09 mA depending on which stage, 3 or 4, is amplifying. Thus, it is shown how the bias current decreases along with the stage position in the pipeline. The AC performance achieved by each one of the two main OTAs is detailed in Table 2.

Fig. 8 shows the measured results for the differential nonlinearity (DNL) and integral nonlinearity (INL). These values are within +1.5/-2 and +2/-1 LSB for a 10 MS/s sampling frequency and 1 kHz of input frequency. Fig. 9 shows the fast Fourier transform (FFT) obtained for a sampling rate and input frequency of 10MS/s and 240 kHz, respectively. The ratio of the root mean square (rms) value of this input signal to the rms value of the worst spurious signals (SFDR) is obtained from Fig. 9 at 960 kHz being its value close to 85 dB. However, this

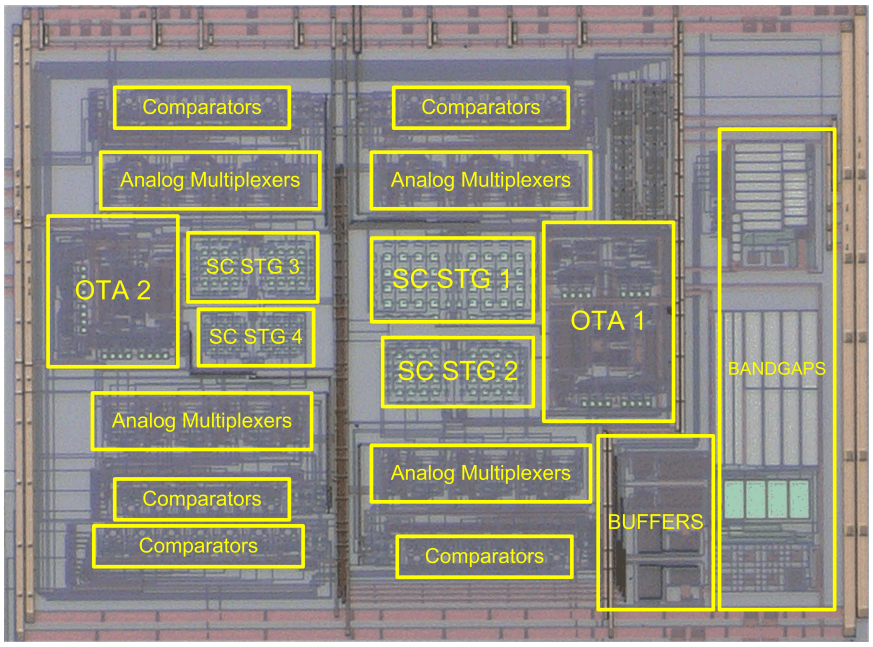

Figure 6: Micrograph of the prototyped chip.

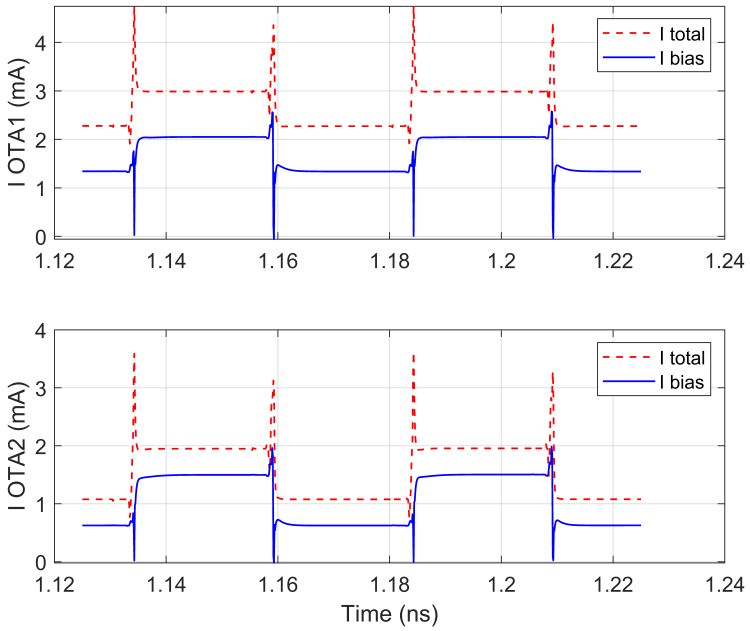

Figure 7: Total current (I_{Total}) and Bias current (I_{Bias}) per OTA with a sampling period of 50 ns.

worst spur has a similar value compared to other spurs located at spurious frequencies. This reveals that other noise sources such as a coupling between digital and analog signals in the real circuit or testing instruments are degrading the ADC performance.

Fig. 10.a shows the measured dynamic performance of the ADC versus input frequency at F_S of 10MS/s. The SNDR remains above 58 dB until an input frequency of 3500 kHz.

Dynamic performance of the ADC versus sampling frequency at F_{IN} of 60 kHz is shown in Fig. 10.b. For low sampling frequencies, the SNDR remains close to 60 dB and it shows a progressive decay for sampling frequency higher than 10 MS/s. The power consumption of the ADC was 17.85 mW for a 3.3V DC power supply with a sampling frequency of 10 MSample/s and input frequency of 2500 kHz excluding PADs and voltage reference circuits. Under these conditions, the power dissipation of the OTAs is 14.55 mW, 77.32% of the overall circuit power consumption. An estimation of the saving in power dissipation using the technique described in this work

Table 2: Summarized AC performance of the OTAs

	OTA 1		OTA 2	
	Stage 1	Stage 2	Stage 3	Stage 4
DC Gain (dB)	89	92	72	84
Unity Gain Freq. (MHz)	529	609	595	628
Phase Margin (Degree)	110	119	108	117
Load Capacitance (pF)	3.36	2.23	1.98	1.06
Input DC voltage (V)	1.2			
Output Swing (V)	2.55-1.05			

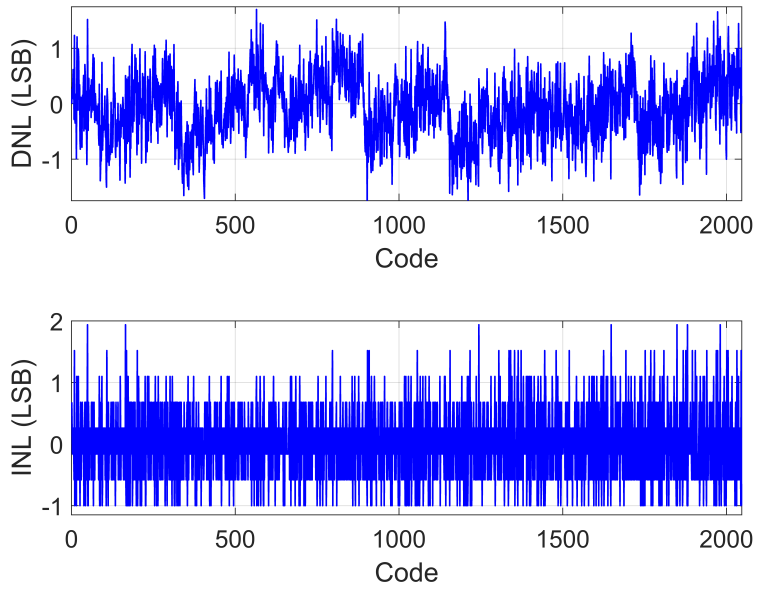

Figure 8: DNL and INL for a 10 MS/s sampling frequency and a low frequency input voltage ramp (1 kHz).

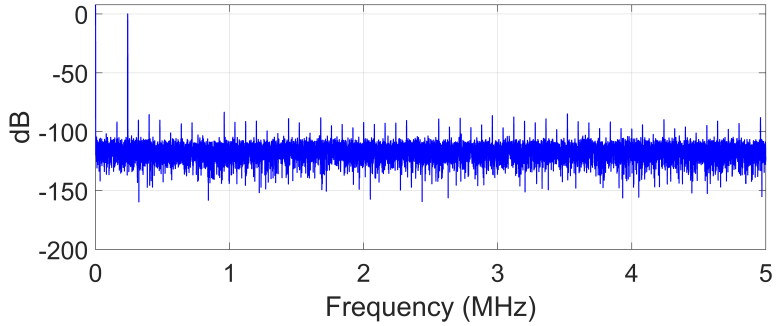

Figure 9: FFT at FS of 10MS/s and $F_{IN} = 240$ kHz

can be obtained from Fig. 7. The bias regulation allows to save 0.72 mA and 0.87 mA respectively for OTA1 and OTA2, which represents an average saving of 16.03 %.

Regarding the silicon area, the current area of stages 1 and 2 is, respectively, 0.1479 mm^2 and 0.1062 mm^2. This includes the OTAs, the switched capacitor circuitry and the multiplexer. If each stage would have its own OTA, the the estimated area would be increased up to 0.1934 mm^2 and 0.1351 mm^2 respectively. This would represent an overall estimated increase of 29.27 % in silicon area.

The Figure of Merit (FoM)[26] defined in 2 under the conditions previously mentioned was 2.64 pJ/step.

$$FoM = \frac{Power}{F_s \cdot 2^{ENOB}} \tag{2}$$

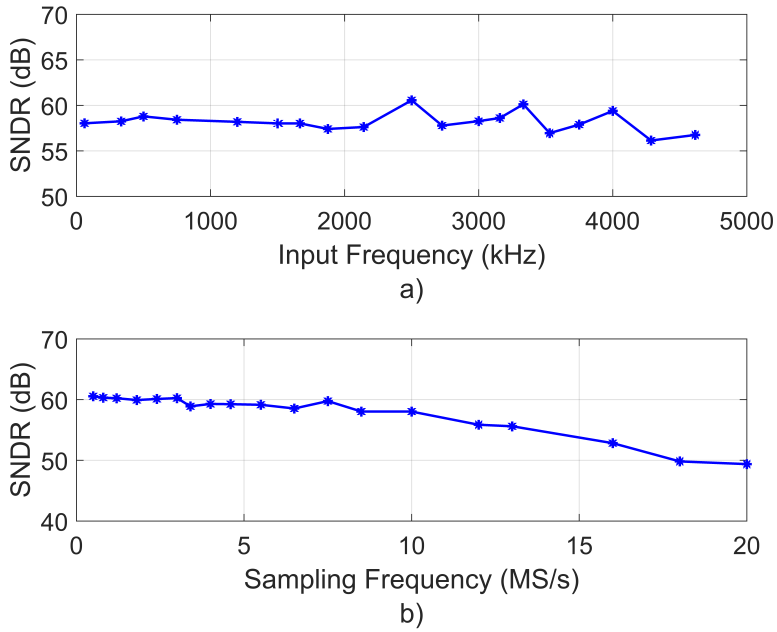

Figure 10: Dynamic performance of the ADC versus a) input frequency at at F_S of 10MS/s and b) sampling frequency at F_{IN} of 60 kHz.

The measured results obtained for the ADC are detailed in Table 3, and compared to other pipelined ADCs prototyped in CMOS 0.35 μm and 0.18 μm technologies. The resolutions of these ADCs are within the range of 10 to 12 bits for sampling rates varying from 10 to 50 Ms/s. The FoM achieved by the proposed circuit is within the range of an order of magnitude compared to the range of FoMs obtained by the rest of the ADCs, although they have been obtained for different values of the input frequency. However, the proposed ADC has the smallest area compared to its technology size. This characteristic can be assessed using the following technological FoM suggested in [4], [5], to compare the power efficiency of different designs prototyped using different technologies:

$$FoM_{TECH} = \frac{Power}{F_s \cdot 2^{ENOB} \cdot L^2 \cdot V_{DD}} \tag{3}$$

where L is the minimum transistor length and V_{DD} is the supply voltage. According to the FoM_{TECH} the proposed ADC shows the best performance when the calibration technique is not considered. Moreover, the ADC described in this work offers the largest input range compared to the voltage supply, which makes it very suitable for low power, large input range and small area implementations.

5 Conclusions

In this paper a low power 11-bit pipelined ADC has been presented. The main novelty of this design is the implementation of an adaptive bias current technique over an amplifier sharing schema. The OTA sharing technique allows a reduction of area while keeping a low power dissipation and the adaptive bias current technique contributes even further to the reduction of power consumption. The prototyped circuit has shown a good performance comparable to other ADCs for a smaller die area and larger input voltage range. In future works, these techniques will be applied to smaller CMOS processes. Given that the reduction in the supply voltage makes the use of a telescopic OTA difficult, other amplifier architectures will be used. Among all the possible architectures, symmetrical or folded-cascode OTA with gain boosting are good candidates because both topologies present a high gain bandwidth, a high output impedance and a wider output voltage range. On the other hand, the use of calibration techniques with the proposed techniques described in this work would allow a higher effective resolution to be reached, improving the overall performance of the ADC. Therefore, the next design will combine these three techniques over a modern CMOS process technology. This ADC would have an effective resolution from 10-14 bit and it could work with sampling rates from 10 to 100 MHz with a low power consumption and effective area. Typical applications that specially require these sampling rates and resolutions are intermediate frequency sampling receivers, software radio receivers and video applications.

Table 3: Summarized performance of the pipelined ADC

Parameter	This work	[6]	[1]	[27]	[30] [a]	[19] [a]
Tech. (μm)	0.35	0.18	0.35	0.35	0.35	0.18
Area (mm^2)	0.95	1.99	1.3	7.5	20.64	0.93
Supply (V)	3.3	1.8	1.5	3.3	3.3	1.8
Resolution (bit)	11	12	10	12	12	12
Samp. Rate (Fs) (MS/s)	10	20	20.48	20	20	50
Power (mW)	17.85	36	19.5	191	56.3	21.6
SNDR@	58.20	66.2	56	67	41.3	60.6
(F_{IN}) (MHz)	1	1		4.7	0.590	60
ENOB (Bits)@	9.38	10.7	9.01	10.83	6.56	-
(F_{IN}) (MHz)	1	1		4.7	0.047	
FoM (pJ/Step)	2.64	1.75	1.85	5.24	29.6	0.49
FoM$_{TECH}$ (As/m^2)	6.53	30	10.06	12.96	73.2	8.4
Input Range (V_{PP})	3	1.2	1	-	2	1.5

[a]Performance without calibration

6 Aknowledgement

This work has been partially funded by Spanish Ministerio de Ciencia e Innovación (MCI), Agencia Estatal de Investigación (AEI) and European Region Development Fund (ERDF/FEDER) under grant RTI2018-097088-B-C33.

References

[1] Adeniran, O.A., Demosthenous, A.: An Ultra-Energy-Efficient Wide-Bandwidth Video Pipeline ADC Using Optimized Architectural Partitioning. IEEE Transactions on Circuits and Systems I: Regular Papers. 53, 2485-2497 (2006)

[2] Arias, J., Boccuzzi, V., Quintanilla, L., Enriquez, L., Bisbal, D., Banu, M., Barbolla, J.: Low-power pipeline ADC for wireless LANs. IEEE J. Solid-State Circuits. 39, 1338–1340, (2004)

[3] Baker, R.J.,: CMOS Mixed-signal circuit design. IEEE Press, Wiley Interscience, New York (2002)

[4] Bechen, B., Boom, T.v.d., Weiler, D., Hosticka, B.J.: Theoretical and practical minimum of the power Consumption of 3 ADCs in SC technique. 18th European Conference on Circuit Theory and Design. Seville, Spain, 444-447 (2007)

[5] Bengt, E.J.: Using Figures-of-Merit to Evaluate Measured A/D-Converter Performance, 2011 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design and IEEE 2011 ADC Forum. Orvieto, Italy, (2011)

[6] Chandrashekar, K., Corsi, M., Fattaruso, J., Bakkaloglu, B.: A 20-MS/s to 40-MS/s Reconfigurable Pipeline ADC Implemented With parallel OTA Scaling. IEEE Transactions on Circuits and Systems II: Express Briefs. 57, 602-606 (2010)

[7] Choi, M.H., Ahn, G.C., Lee, S.H,: 12b 50 MSs 0.18 μm CMOS ADC with highly linear input variable gain amplifier. Electronics Letters. 46, 1254-1256 (2010)

[8] Choksi, O., Carley, L. R.: Analysis of switched-capacitor common-mode feedback circuit. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. 50, 906-917 (2003)

[9] Cline, D.W., Gray, P.R.: A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS. IEEE J. Solid State Circuits. 31, 294-303 (1996)

[10] Diaz-Madrid, J-A, Domenech-Asensi, G, Hauer, J, Mateu, L. A low kickback fully differential dynamic comparator for pipeline analog-to-digital converters. Engineering Reports. (2019)

[11] Díaz-Madrid, J.A., Domenech-Asensi, G., Lopez-Alcantud, J.A., Oberst, M.: An 11-bit 20-MSample/s pipelined ADC with OTA bias current regulation to optimize power dissipation. IEEE Intl. Symposium on Circuits and Systems (ISCAS). Baltimore, USA, 1-4 (2017)

[12] Diaz-Madrid, J.A., Neubauer, H., Hauer, H., Domenech-Asensi, G., Ruiz-Merino, R.: Power reduction of a 12-bit 40-MS/s pipeline ADC exploiting partial amplifier sharing. Design, Automation & Test in Europe Conference & Exhibition. Nice, France, 369-373 (2009)

[13] Fang, B., Wu, J.: A 10-Bit 200-MSs digitally-calibrated pipelined ADC using switching opamps. IEEE International Symposium on Circuits and Systems (ISCAS). Seoul, South Korea, 1042-1045 (2012)

[14] Goes, J., Vital, J.C., Franca, J.E.: Systematic design for optimization of high-speed self-calibrated pipelined A/D converters. IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. 45, 1513-1526 (1998)

[15] Jia, H., Chen, G., Zhang, H.: A Low Power 12-bit 40MSs Pipelined ADC with Digital Calibration. APCCAS IEEE Asia Pacific Conference on Circuits and Systems. Macao, China, 137-140 (2008)

[16] Jin, W., Yulin, Q.: Analysis and design of fully differential gain-boosted telescopic cascode opamp. Proc. of 7th Intl. Conf. on Solid-State and Integrated Circuits Technology. 1457-1460 (2004)

[17] Kurose, D., Ito, T., Ueno, T., Yamaji, T., Itakura,T.:55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receiver. IEEE Journal of Solid State Circuitsl. 41, 1589-1595 (2006)

[18] Kwok, P.T.F., Luong, H.C.: Power optimization for pipeline analog-to-digital converters. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. 46, 549-553 (1999)

[19] Lee, K. H., Kim., K.S., Lee, S.H.: A 12b 50 MS/s 21.6 mW 0.18 um CMOS ADC Maximally Sharing Capacitors and Op-Amps. IEEE Transactions on Circuits and Systems I: Regular Papers. 58, 2127-2136 (2011)

[20] Lee, B., Tsang, R.M.: A 10-bit 50 MS/s Pipelined ADC With Capacitor-Sharing and Variable-g_m Opamp. IEEE Journal of Solid-State Circuits. 44, 883-890 (2009)

[21] Mehr, I., Singer, L.: A 55-mW, 10-bit, 40-Msample/s Nyquist-rate CMOS ADC. IEEE Journal of Solid-State Circuits, 35, 318-325 (2000)

[22] Min, B.M., Kim, P., Bowman, F.W., Boisvert, D.M., Aude, A.J.: A 69-mW 10-bit 80-MSample/s pipelined CMOS ADC. IEEE J. Solid State Circuits. 38, 2031–2039 (2003)

[23] Park, Y.I., Karthikeyan, S., Tsay, F., Bartolome, E.:A 10 b 100 MSample/s CMOS pipelined ADC with 1.8 V power supply: IEEE International Solid-State Circuits Conference. Digest of Technical Papers. San Francisco, CA, USA, 130-131 (2001)

[24] Ruiz-Amaya, J., Delgado-Restituto, M., Rodriguez-Vazquez, A.: Transistor-Level Synthesis of Pipeline Analog-to-Digital Converters Using a DesignSpace Reduction Algorithm. IEEE Transactions on Circuits and Systems I: Regular Papers. 58, 2816-2828 (2011)

[25] Ruiz-Amaya, J., Delgado-Restituto, M., Rodríguez-Vázquez, A.: Device-Level Modeling and Synthesis of High-Performance Pipeline ADCs. Springer, Berlin (2011)

[26] Walden, R.H..: Analog-to-Digital Conversion in the Early Twenty-First Century. Wiley Encyclopedia of Computer Science and Engineering, 126–138 (2008)

[27] Wang, H., Wang, X., Hurst, P.J., Lewis, S.H.: Nested Digital Background Calibration of a 12-bit Pipelined ADC Without an Input SHA. IEEE Journal of Solid-State Circuits. 44, 2780-2789 (2009)

[28] Yasue, T., et al.,: A 33 Mpixel CMOS imager with multi-functional 3-stage pipeline ADC for 480fps high-speed mode and 120fps low-noise mode. IEEE International Solid - State Circuits Conference - (ISSCC). San Francisco, CA, 90-92 (2018)

[29] Yu, P.C., Lee, H.S.: A 2.5-V, 12-b, 5-MSample/s pipelined CMOS ADC. IEEE J. Solid-State Circuits. 31, 1854–1861 (1996)

[30] Yuan, J., Fung, S.W., Chan, K.Y., Xu, R.: A 12-bit 20 MS/s 56.3 mW Pipelined ADC With Interpolation-Based Nonlinear Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers. 59, 555-565 (2012)